REMARKS

Claims 1-19 and 21-28 are pending in this application, of which claim 1 has been amended. Claim 20 has been cancelled. Claims 3, 6, and 22-28 are withdrawn from consideration. No new claims have been added.

Rejections under 35 USC §103(a)

Claims 1, 2, 4, 5, 7-9 and 13-16 were rejected under 35 USC §103(a) as being unpatentable over Domae (US Publication Application No. 2002/0005584).

Claim 1 has been amended to recite "said first multilayer interconnection structure including a pillar vertically extending straight from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar being formed in a region of said substrate right underneath an electrode pad so as to support stress during wire bonding."

Domae describes the semiconductor device as follows:

> [0011] In consideration of the aforementioned problems, a first object of the invention is realizing both decrease of the RC delay time and **increase of the mechanical strength** of a pad region, and a second object is realizing both decrease of the RC delay time and improvement of the heat conducting property of a power line region.
> [0012] In order to achieve the first object, the first semiconductor device of this invention comprises an interlayer insulating film formed from a **first insulating material** between a lower interconnect layer and an upper interconnect layer in a pad region on a semiconductor substrate; and an interconnect insulating film formed from a **second insulating material** between adjacent interconnects in an interconnect layer in a signal delay preventing region on the semiconductor substrate, and **the first insulating material has higher mechanical strength** than the second insulating

> material, and **the second insulating material has a lower dielectric constant** than the first insulating material.

Although Domae mentions "increase of the mechanical strength of a pad region," it is achieved by a combination of an interlayer insulating film formed from a first insulating material having higher mechanical strength and an interconnect insulating film formed from a second insulating material having a lower dielectric constant. Regarding Fig. 4, which is referred to by the Office Action, Domae describes as follows:

> [0114] Power lines formed adjacent to each other in the vertical direction and set to the same potential are **connected to each other through a via 109**, and signal lines formed adjacent to each other in the vertical direction and transferring the same signal are connected to each other through a via 109.

Although Fig. 4 may appear to show a pillar vertically extending straight from a surface of the substrate and reaching at least the second multilayer interconnection structure, Domae simply indicates that the power lines formed adjacent to each other in the vertical direction are connected to each other through a via 109, but **does not discuss the interconnection structure including a pillar**.

Moreover, Fig. 4 shows via 109 which is thinner than via extending from the surface of the substrate. Also, the pillar vertically extending straight is positioned at the side of the bonding pad. These indicate that the pillar is not intended to support stress during wire bonding. Also,

the structure which appears to include a pillar vertically extending merely is meant to schematically show the vertical connection, but not a pillar being formed in a region of said substrate right underneath an electrode pad **so as to support stress during wire bonding.**

Vigna et al describes at the cited portion as follows:

> As will be noted, at the bottom, pad 28 is connected to a bearing structure 31 comprising regions 21, 15a and portions 24, 19, 12 and extending vertically entirely outside the component 3; in particular, on one side, the bearing structure 31 electrically connects the pad 28 to component 3 through portion 15b and on the other side it acts to **concentrate the mechanical stress to which the pad is subjected during wire bonding on a limited peripheral** area not containing electronic components or conductive regions, but only field oxide layer 6. In this way the stress exerted on component 3 during wire bonding is considerably reduced; furthermore, there are no dielectric/metal interfaces between second and third metal layers 18, 23 on top of component 3; consequently, delamination problems are eliminated in this zone.

(Vigna et al, column 3, lines 22-36). According to Vigna et al, the mechanical stress is concentrated on the peripheral area which is outside of the actual bonding pad. Thus, the structure necessarily becomes complex. In contrast, according to the present invention by positioning the pillar right underneath an electrode pad so as to support stress during wire bonding the structure can be simplified.

Thus, Domae and Vigna et al do not teach or suggest, among other things, "said first multilayer interconnection structure including a pillar vertically extending straight from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar

being formed in a region of said substrate right underneath an electrode pad so as to support stress during wire bonding."

For at least these reasons claim 1 patentably distinguishes over Domae and Vigna et al. Claims 2, 4, 5, 7-9 and 13-16, depending from claim 1, also patentably distinguish over Domae and Vigna et al for at least the same reasons.

Claims 10-12 and 17-19 were rejected under 35 USC §103(a) as being unpatentable over Domae (US Publication Application No. 2002/0005584) in view of Vigna et al. (U.S. Patent No. 6,605,873) as applied to claim 1 above, and further in view of the Applicant's Prior Art Figures 1-4 (APAF).

Claims 10-12 and 17-19 depend from claim 1.

Applicant's Figures 1-4 have been cited for allegedly disclosing the first and second interlayer insulating films each having a desired Young's Modulus. However, such disclosure of the present specification and drawings does not remedy the deficiencies of Domae and Vigna et al as discussed above.

For at least these reasons claims 10-12 and 17-19 patentably distinguish over Domae, and Vigna et al and alleged prior art.

Moreover, the present specification discusses Figs. 1-4 simply as related art, which are not admitted to be the prior art.

Claim 21 was rejected under 35 USC §103(a) as being unpatentable over Domae (US Publication Application No. 2002/0005584) in view of Vigna et al. (U.S. Patent No. 6,605,873) as applied to claim 1 above, and further in view of Sugiyama et al. (US Publication Application No. 2002/0040986).

Sugiyama et al has been cited for allegedly disclosing "wherein said pillar is provided in plural number on said substrate, and wherein there is formed a reinforcement structure in said first multilayer interconnection structure so as to extend diagonally between said plural pillars."

However, such disclosure of the present specification and drawings does not remedy the deficiencies of Domae and Vigna et al as discussed above.

For at least these reasons claim 21 patentably distinguishes over Domae, and Vigna et al and Sugiyama et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned representative at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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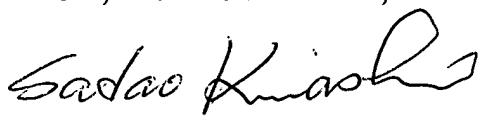

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Attachment: Petition for Extension of Time